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Claim Amendments

Please amend claims 1, 10, 12, and 20 as follows:

Please cancel claims 9 and 19 as follows:

Listing of Claims

1. (currently amended) A method for forming a single transistor planar RAM memory cell with improved charge retention comprising the steps of:

providing a silicon substrate comprising an STI structure and an overlying dielectric gate layer;

depositing a polysilicon layer;

forming a pass transistor structure adjacent a planar storage capacitor structure separated by a predetermined distance;

carrying out a first ion implantation process to form first and second P- doped regions adjacent either side of the pass transistor structure, the first doped region defined by the predetermined distance;

depositing a spacer dielectric layer;

etching back the spacer dielectric layer to ~~leave an unetched spacer dielectric layer portion overlying~~ form an ion implant mask fully covering the first doped region while forming a sidewall spacer of a predetermined width overlying a first portion of the second doped region;

wherein the predetermined distance is less than ~~about~~ twice the predetermined width; and,

carrying out a second ion implantation process to form a ~~relatively higher dopant concentration~~ P+ doped region in a second portion of the second doped region while retaining the P- doped region in the first doped region.

2. (original) The method of claim 1, further comprising the step of forming self aligned silicide regions over the second portion, the pass transistor structure and the storage capacitor structure.

3. (original) The method of claim 1, wherein the dielectric gate layer is selected from the group consisting of SiO_2, nitrided

SiO_2, and oxide/nitride.

4. (original) The method of claim 1, wherein the dielectric gate layer comprises material selected from the group consisting of Ta_2O_5, TiO_2, HfO_2, Y_2O_3, La_2O_5, ZrO_2, BST, and PZT.

5. (original) The method of claim 1, wherein the storage capacitor structure is formed at least partially overlying the STI structure.

6. cancelled

7. (original) The method of claim 1, wherein the spacer dielectric layer thickness is about greater than about half of the predetermined distance.

8. (original) The method of claim 1, wherein the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region of a P doped silicon

substrate.

9. cancelled

10. (currently amended) The method of claim 1, wherein the ~~first~~ P- doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the second P+ doped region ~~comprises a relatively higher doped region of~~ is doped to a level greater than about 10^{15} dopant atoms/cm^2.

11. (original) The method of claim 1, wherein the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

12. (currently amended) A method for forming a single transistor planar RAM memory cell with improved charge retention comprising the steps of:

providing a silicon substrate comprising an STI structure and an overlying dielectric gate layer;

depositing a polysilicon layer;

forming a pass transistor structure adjacent a planar storage capacitor structure separated by a predetermined distance for forming a first doped region;

carrying out a first ion implantation process to form the first doped region and a second doped region to form P-doped regions adjacent the pass transistor structure;

blanket depositing a spacer dielectric layer having a thickness about greater than the predetermined distance to substantially fill a space between the pass transistor structure and the storage capacitor structure;

etching back the spacer dielectric layer to ~~leave an unetched spacer dielectric layer portion overlying~~ form an ion implant mask fully covering the first doped region while forming a sidewall spacer overlying a first portion of the second doped

region;

wherein the predetermined distance is less than ~~about~~ twice the sidewall spacer width; and,

carrying out a second ion implantation process to form a relatively higher dopant concentration to form a P+ doped region in a second portion of the second doped region while retaining the P- doped region in the first doped region.

13. (original) The method of claim 12, further comprising the step of forming salicide regions over the second portion, the pass transistor structure and the storage capacitor structure.

14. (original) The method of claim 12, wherein the dielectric gate layer is selected from the group consisting of SiO_2, nitrided SiO_2, and oxide/nitride.

15. (original) The method of claim 12, wherein the dielectric gate layer comprises material selected from the group consisting

of Ta_2O_5, TiO_2, HfO_2, Y_2O_3, La_2O_5, ZrO_2, BST, and PZT.

16. (original) The method of claim 12, wherein the storage capacitor structure is formed at least partially overlying the STI structure.

17. cancelled

18. (original) The method of claim 12, wherein the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region of a P doped silicon substrate.

19. cancelled

20. (currently amended) The method of claim 12, wherein the ~~first~~ P- doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the ~~second~~ P+ doped region ~~comprises a relatively higher doped region of~~ is doped to a level greater than about 10^{15} dopant atoms/cm^2.

21. (original) The method of claim 12, wherein the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

claims 22-32 cancelled